

**REMARKS**

Claims 1-5 are pending. Claim 5 is added.

Claims 1 and 2 were rejected under 35 USC §102(b) as anticipated by or, in the alternative, under 35 USC §103(a) as obvious over Ehman et al. The Examiner notes that Ehman et al. discloses bonding of layers 12, 14 and 16 to each other by intermediate layers 18 and 20 (B-stage thermal setting resin (See column 2, lines 54-56)). This rejection is respectfully traversed.

As disclosed in column 2, lines 42-67, and Fig. 1 and Fig. 2 of Ehman, in the multilayer printed circuit board 10 layers 12, 14 and 16 are fabricated in advance with electronic components embedded therein. When fabricating the multilayer printed circuit board 10, the layers 12, 14 and 16 are bonded to each other with intermediate layers 19, 20. Fig. 2 shows the electronic components inside the layer 14.

In contrast, according to claim 1 of the present invention, the frame resin layer 11 does not contain any electronic components. When fabricating the multilayer wiring board of the present invention, electronic components are placed on the surface of the frame resin layer 11, and then the resin layer 12 is placed on the surface of the frame resin layer 11 to bury the electronic components. In this way, the multilayer wiring board of the present invention is fabricated.

Claims 1 and 2 were also rejected under 35 USC §103(a) as being unpatentable over Takanaka et al. (JP' 868) in view of Ehman et al. In this rejection, the Examiner applies Takanaka et al. as a primary reference.

In this rejection, it appears that the Examiner acknowledges that Takanaka et al. does not teach the claimed first step of mounting an electronic component on a frame resin layer including at least one of glass cloth, filler and non-woven fabric, said frame resin layer including no electronic component therein. Ehman et al. is applied by the Examiner for teaching mounting of electronic components on a resin layer. The Examiner concludes that it would have "been obvious to one of ordinary skill in this art to combine the two teachings and to provide electronic components on the substrate by Takanaka et al. rather than circuits and thereafter completely cure the semi-cured sheet with the electronic components buried therein." This rejection is respectfully traversed.

In the first instance, the Examiner has failed to provide any reasoning why it would have been obvious to combine the references in a manner suggested by the Examiner. The Examiner merely states that it would have been obvious to combine the teachings to obtain the claimed invention, without providing any reasoning why one of ordinary skilled in the art would have been motivated to combine the references. The rejection should not stand unless the Examiner can provide a showing of motivation by either of the references to make the modifications asserted by the Examiner.

Amendment  
Serial No. 10/664,928  
Attorney Docket No. 021385A

Furthermore, it does not appear that one of ordinary skill in the art would have even considered combining the references as suggested by the Examiner. Takanaka et al. appears to be directed to merely laminating prepreg sheets 1a, 1b on opposing sides of a circuit board, not a frame resin layer. There appears to be no reason why one of ordinary skill in the art would look to Ehman et al. and have been motivated to replace the circuit board of Takanaka et al. with mounting electronic components on a resin layer of Ehman et al.

New claim 5 has been added. Claim 5 sets forth an additional step of forming wiring patterns on the cured resin layer. Such a step would not be possible for the layers 18 and 20 of Ehman et al. since Ehman et al.'s layer is used for bonding.

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

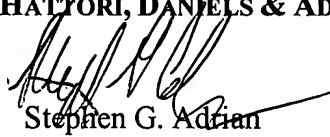
Should the Examiner deem that any further action by applicant would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicant's undersigned attorney.

Amendment  
Serial No. 10/664,928  
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If this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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